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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/785,006	SCHOENFELD, AARON	
	Examiner	Art Unit	
	Evan Pert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-25,35-39 and 41-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-25,35-39 and 41-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11-25, 35-39, and 41-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Indefinite - "reduced width"

All of the claims include the limitation that circuitry on a semiconductor die is "surrounded by an unused *reduced width* buffer area." Since the pending claims are product claims, not process claims, the claimed "reduced width" is an ambiguous "width." For example, a one-foot-square piece of wood "reduced from a 5 foot square" looks the same as a one-foot-square piece of wood "reduced from any size larger than one-foot-square." For purposes of examination, the "reduced width" is considered as being a "width."

Indefinite – "ground" or "polished"

All of the claims include the limitation that a side surface of a semiconductor die is "ground" or "polished." However, the term "ground (or polished)" in claims 11, 14, 15, 18, 19, 22, 25, 35, 39 and 41 is a relative term, which renders the pending claims indefinite. The term "ground (or polished)" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the "semiconductor die" invention.

Applicant uses the word "ground" to mean "treated by grinding the side surface of the die after dicing the die out of a wafer," so the claimed "semiconductor die" has an edge that is claimed to be "ground." However, any prior art semiconductor die cut by a dicing blade *inherently* "has a ground surface" [Weisshaus et al., p. 30, left column].

Applicant's use of "ground" in the claims is ambiguous because scope of claimed surface roughness is not *quantified*, and dicing a prior art die inherently results in a "ground" side surface when using a dicing saw [Weisshaus et al., p. 30, left column].

For purposes of examination, a "ground" side surface of a semiconductor die *inherently* exists when the die was cut with a dicing saw blade, regardless of the quantifiable degree of roughness of the grinding cut.

Indefinite – "without substantially any..."

The term "without substantially any irregularities that produce weak points in the substrate" in claims 11, 15, 18, 22, 25, 35 and 41 is a relative term which renders the claims indefinite. The term "without substantially any" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

For purposes of examination, any semiconductor die that "has substantially smooth edge surfaces and uniform dimensions" or has "a high quality side face surface which does not need polishing" is considered to fall within the scope of a semiconductor die that has a side surface claimed as "without substantially any irregularities that produce weak points in the substrate."

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-16, 18-25, 35-38, and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 0 678 904 A1 (Boruta) in view of US 3,545,325 (Camasta), US 3,689,803 (Baker et al.), and Weisshaus et al. (Dicing article).

The secondary reference to Weisshaus et al. does not antedate applicant's effective filing date, and is relied on only for teaching the *universal fact* that a semiconductor die's side surface is a "ground surface" when the die is cut from a semiconductor wafer with a dicing saw blade [see MPEP 2124].

The secondary reference to Baker et al. is cited for teaching that it is old in the art to provide a width of buffer area around active circuitry on a semiconductor die, the width of the buffer area being chosen depending on the distance edge defects may extend (i.e. smaller and smaller edge defects implies smaller and smaller width needed for a buffer area around active circuitry). See col. 1, lines 39-57.

The secondary reference to Camasta is cited for teaching a dicing apparatus that produces semiconductor die that "have substantially smooth edge surfaces and uniform dimensions" with "substantial elimination of rough edges, broken corners and varying dimensions..."

The primary reference to Boruta discloses semiconductor die that have active circuitry on a first planar surface opposite a second planar surface (i.e. active circuitry on the side with test circuitry in the dicing lanes), with side surfaces having bi-level (comparing Species I to Fig 2D of Boruta) and flat (comparing Species II to 1B of Boruta) configurations, meeting all of the wordy limitations drawn to *relative orientation* of "surfaces" of semiconductor die with bi-level (i.e. claims 18, 20-25, 35, 36, 38, 41 and 43) and flat (i.e. claims 11, 12, 15, 16) side surfaces.

Boruta does not disclose "an unused width of buffer area around active circuitry on the semiconductor die" as is old in the art. However:

Baker et al. explains that "a width of buffer area is set in accordance with the distance an edge defect in the chip resulting from handling and usually from dicing may extend from the edge into the chip. This minimum distance is most desirably beyond the point to which such edge defects may extend" [col. 1, lines 39-57].

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to include a width of buffer area around active circuitry of die in Boruta, motivated to avoid damage to active circuitry from an edge defect as known in the art per Baker et al., with Baker et al. explaining that the width of the buffer area is dependent on the edge defect severity for a given dicing process.

Boruta does not disclose that side surfaces of diced die of their invention are "ground or polished" surfaces "without substantially any irregularities that produce weak points in the substrate." However:

Camasta discloses a dicing apparatus that inherently results in a "ground" side surface from the grinding action of the blade [i.e. universal fact disclosed in Weisshaus et al.]. Furthermore, the dicing apparatus of Camasta "is capable of cutting chip devices from a wafer so that the chip devices have substantially smooth edge surfaces and uniform dimensions," wherein the dicing apparatus "substantially eliminates the rough edges, broken corners..." [col. 4]

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt the dicing apparatus of Camasta for practicing the dicing method of Boruta. One of ordinary skill in the art would have been motivated to adopt the dicing apparatus of Camasta for practicing the method of Boruta because the apparatus "substantially eliminates" undesirable imperfections that "could affect the operation of subsequent handling operations of the chip devices" [cols. 1 and 4].

Since the dicing of Camasta "substantially eliminates" undesirable imperfections at the die edge with an apparatus that "is capable of cutting chip devices from a wafer so that the chip devices have substantially smooth edge surfaces and uniform dimensions," and the apparatus necessarily yields "ground surfaces" at side surfaces of dice [Weissman et al.], the practice of Boruta's dicing method using Camasta's dicing apparatus necessarily results in ground side surfaces "without substantially any irregularities that produce weak points in the substrate," at least to the degree of clarity offered by applicant's ambiguous disclosure [see rejection under 35 USC 112, 2nd paragraph above].

Regarding claims 13, 19, 37 and 42, each of the die are rectangular, as is known to the most rudimentary of skill in the art, because the scribe lines are perpendicular (see, for example, Figures 5, 6 and 7 of Camasta).

3. Claims 17 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 0 678 904 A1 (Boruta) in view of US 3,545,325 (Camasta et al.), US 3,689,803 (Baker et al.), and Weisshaus et al. (Dicing article), as applied to claims 15 and 35 above, and further in view of US 5,408,739 (Altavela et al.).

All of the claims except claims 17 and 39 include the limitation of a side surface of a semiconductor die having a "ground or polished surface," wherein claims 17 and 39 further limit "ground or polished" to be specifically "polished."

Altavela et al. teach that a "dicing cut" made with "a resin blade" is "well known in the art of semiconductor dicing and can provide a very high quality [side] surface 90 which does not need further processing, such as polishing" [col. 6, lines 55-65].

Thus, Altavela et al. teach that a "resin blade" results in a surface that is indistinguishable from an ambiguously claimed "polished surface" because a cut surface from a "resin blade" does "not need to be polished."

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt "resin blades" in the blade pack of Camasta, for practicing the dicing method of Boruta.

One of ordinary skill in the art of semiconductor dicing would have been motivated to eliminate imperfections at the side surfaces of a cut die per Camasta (col. 1, lines 13-15), by using "resin blades," because a resin blade results in "a very high quality" side surface with "does not need to be polished." Since the side surfaces of the die do "not need to be polished," they are necessarily indistinguishable from applicant's ambiguously claimed "polished" sides [see rejection under 35 USC 112 above].

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ETP
December 7, 2004

EVAN PERT
PRIMARY EXAMINER